Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Previously Presented) A switching apparatus comprising:

a first port coupled to receive an input data frame;

a first logic circuit coupled to receive the input data frame from the first port and configured to determine a number of copies of the input data frame to make and to make the number of copies of the input data frame;

a first memory comprising multiple segments, each segment comprising multiple independently addressable channels, the first logic circuit configured to determine a number of channels and segments needed to store the number of copies of the input data frame, the first memory coupled to the first logic circuit and configured to store multiple copies of the input data frame within a single segment of the determined number of segments and to read the multiple copies of the input data frame from the single segment in a single read cycle; and

multiple transmitting ports coupled to the first memory and configured to receive copies of the input data frame from the first memory in parallel and to simultaneously transmit the copies of the input data frame, each of the multiple transmitting ports associated with an output control logic circuit coupled to the first memory and configured to determine when to read at least one copy of the input data frame from the first memory;

wherein the first logic circuit further comprises a third logic circuit configured to determine one or more empty locations in the first memory to store the copies of the input data frame.

2. (Canceled).

3. (Previously Presented) The switching apparatus of claim 1 wherein the first logic circuit further comprises a second memory configured to keep track of all of the empty locations in the first memory.

4. (Previously Presented) The switching apparatus of claim 3 wherein: the third logic circuit is configured to determine where there are empty channels in the first memory to store the copies of the input data frame.

5. (Previously Presented) The switching apparatus of claim 3 wherein: the third logic circuit is configured to determine where there is at least one empty segment in the first memory to store one of the copies of the input data frame.

6. (Canceled)

7. (Previously Presented) The switching apparatus of claim 1 wherein: the third logic circuit is configured to determine how many additional ports will output some of the copies of the input data frame and to calculate the minimum amount of storage space

that is necessary to store all of the necessary copies of the input data frame in the first memory.

8. (Previously Presented) The switching apparatus of claim 1 wherein the first logic circuit further comprises a fourth logic circuit configured to determine the size of the input data frame such that the size of the input data frame is used to calculate the minimum amount of storage space necessary to store the copies of the input data frame.

9. (Canceled)

10. (Previously Presented) The switching apparatus of claim 1 wherein the first memory is distributed across the switching apparatus.

11. (Previously Presented) The switching apparatus of claim 1 further comprising a bus coupled with the first memory and one or more transmitting ports and configured to transmit data including at least one copy of the input data frame from the first memory to the one or more transmitting ports.

12. (Previously Presented) The switching apparatus of claim 11 wherein one or more transmitting ports comprises a logic circuit configured to select the at least one copy of the input data frame from the bus.

13. (Previously Presented) The switching apparatus of claim 1 wherein at least one output control logic circuit is further configured to indicate a location in the first memory where an associated transmitting port is to obtain the at least one data frame for transmitting.

14. (Previously Presented) A switching apparatus comprising:

a first logic circuit coupled to receive an input data frame and configured to determine a number of copies of the input data frame to make and to make the determined number of copies of the input data frame;

a memory coupled to the first logic circuit and configured to store and read the copies of the input data frame, the memory being comprised of segments including independently addressable channels with one or more segments being accessible at a given time, the first logic circuit configured to determine a number of channels and segments needed to store the number of copies of the input data frame, the first memory to store multiple copies of the input data frame within a single segment of the determined number of segments and to read the multiple copies of the input data frame from the single segment in a single read cycle; and

multiple transmitting ports coupled to the first memory and configured to receive copies of the input data frame from the first memory in parallel and to simultaneously transmit the copies of the input data frame, each of the multiple transmitting ports associated with an output control logic circuit coupled to the memory and configured to determine when to read at least one copy of the input data frame from the memory;

wherein the first logic circuit further comprises a third logic circuit configured to determine one or more empty locations in the memory to store the copies of the input data frame.

15. (Canceled).

16. (Previously Presented) The switching apparatus of claim 14 wherein the third logic circuit is configured to determine where there are empty channels in the memory for storing copies of the input data frame.

17. (Previously Presented) The switching apparatus of claim 14 wherein the third logic circuit is configured to determine where there is at least one empty segment in the memory for storing at least one copy of the input data frame.

18. (Previously Presented) The switching apparatus of claim 14 wherein the third logic circuit is configured to determine how many of the multiple transmitting ports will output some of the number of copies of the input data frame and to calculate the minimum amount of storage space necessary to store all of the necessary copies of the input data frame in the memory.

19. (Original) The switching apparatus of claim 14 wherein the first logic circuit further comprises a fourth logic circuit configured to determine the size of the input data frame in calculating the minimum amount of storage space to store the necessary copies

of the input data frame in the memory.

20. (Canceled)

21. (Previously Presented) A switching apparatus comprising:

a first port coupled to receive an input data frame;

a memory coupled to the first port and configured to store and read a number of copies of the input data frame, the memory comprising multiple segments, each segment comprising multiple independently addressable channels;

a processor coupled to the memory and programmed to determine the number of copies of the input data frame to make and to determine when to read at least one copy of the input data frame from the memory, the processor configured to determine a number of channels and segments needed to store the number of copies of the input data frame, the memory to store multiple copies of the input data frame within a single segment of the determined number of segments and to read the multiple copies of the input data frame from the single segment in a single read cycle; and

multiple transmitting ports coupled to the memory and configured to receive copies of the input data frame from the first memory in parallel and to simultaneously transmit the copies of the input data frame after being read from the memory;

wherein the processor is configured to determine one or more empty locations in the memory to store the copies of the input data frame.

22. (Canceled).

23. (Previously Presented) The switching apparatus of claim 21 wherein the processor determines where there are empty channels in the memory to store the number of copies of the input data frame.

24. (Previously Presented) The switching apparatus of claim 21 wherein the processor determines where there is at least one empty segment in the memory to store the number of copies of the input data frame.

25. (Canceled)

26. (Previously Presented) The switching apparatus of claim 21 wherein the processor determines how many transmitting ports will output any of the copies of the data frame and calculates a minimum amount of storage space necessary to store the copies of the input data frame.

27. (Original) The switching apparatus of claim 26 wherein the processor determines the size of the input data frame and uses this determination in calculating the minimum amount of storage space to store the number of copies of the input data frame.

28. (Canceled)

29. (Previously Presented) A computer readable medium for use in a switching apparatus that includes a processor, the computer readable medium including instructions for causing the processor to:

determine a number of ports a received data frame is to be transmitted out over so as to generate a same number of copies of the received data frame;

determine particular locations in a memory that can store the copies of the received data frame;

determine a number of channels and segments needed to store the number of copies of the input data frame;

forward instructions and the copies of the received data frame to the memory so as to cause the memory to store multiple copies of the received data frame within a single segment of the determined number of segments;

forward instructions to the memory to read out the multiple copies of the received data frame from the single segment in parallel and output the copies onto a bus in a single clock cycle;

forward instructions to multiple transmitting ports causing the multiple transmitting ports to retrieve and simultaneously transmit the copies of the received data frame from the bus; and

determine one or more empty locations in the memory to store the copies of the input data frame.

30. (Previously Presented) The computer readable medium of claim 29 wherein the processor is instructed to determine the location or locations, addressable by channels and

segments, that can store the copies of the received data frame.

31. (Previously Presented) The computer readable medium of claim 30 further comprising an instruction for the memory to store some copies of the received data frame in multiple segments of the memory.

32. (Original) The computer readable medium of claim 30 wherein when the memory reads out at least one copy of the number of copies of the received data frame, the memory also reads out a previously stored copy from a previously received data frame.

33. (Original) The computer readable medium of claim 29 wherein the instructions cause the processor to determine the size of the received data frame and use a result from this determination when the processor is determining particular locations in the memory to store the copies of the received data frame.